Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

Claim 1-121. (canceled)

122. (new) An electronic component comprising:

multiple I/O circuits;

an interconnecting structure;

a passivation layer over said interconnecting structure; and

an upper interconnecting structure over said passivation layer and connecting said multiple I/O circuits.

123. (new) The electronic component of Claim 122, wherein said passivation layer comprises a topmost nitride layer.

124. (new) The electronic component of Claim 122, wherein said passivation layer comprises a topmost oxide layer.

125. (new) The electronic component of Claim 122, wherein said passivation layer comprises a topmost CVD insulating layer.

126. (new) The electronic component of Claim 122, wherein said upper interconnecting structure comprises a signal bus connecting said multiple I/O circuits.

127. (new) The electronic component of Claim 126, wherein said signal bus is used to transmit address signals.

128. (new) The electronic component of Claim 126, wherein said signal bus is used to transmit data signals.

129. (new) The electronic component of Claim 126, wherein said signal bus is used to transmit logic signals.

130. (new) The electronic component of Claim 126, wherein said signal bus is used to transmit analog signals.

131. (new) The electronic component of Claim 126, wherein said signal bus is used to transmit clock signals.

132. (new) The electronic component of Claim 126, wherein said signal bus is used to transmit a power voltage.

133. (new) The electronic component of Claim 126, wherein said signal bus is used to transmit a ground voltage.

134. (new) The electronic component of Claim 122 further comprising an external connection connected to one of said multiple I/O circuits.

135. (new) The electronic component of Claim 134 further comprising an ESD circuit connected to said external connection.

136. (new) The electronic component of Claim 122 is a semiconductor chip.

137. (new) The electronic component of Claim 122 is a semiconductor wafer.

138. (new) The electronic component of Claim 122, wherein said multiple I/O circuits comprise a receiver.

139. (new) The electronic component of Claim 122, wherein said multiple I/O circuits comprise a driver.

140. (new) An electronic component comprising:

a semiconductor circuit;

a first I/O circuit;

a second I/O circuit;

an interconnecting structure connecting said semiconductor circuit and said first I/O circuit;

a passivation layer over said interconnecting structure; and

an upper interconnecting structure over said passivation layer and connecting said first and second I/O circuits.

141. (new) The electronic component of Claim 140, wherein said passivation layer comprises a topmost nitride layer.

142. (new) The electronic component of Claim 140, wherein said passivation layer comprises a topmost oxide layer.

143. (new) The electronic component of Claim 140, wherein said passivation layer comprises a topmost CVD insulating layer.

144. (new) The electronic component of Claim 140, wherein said upper interconnecting structure comprises a signal bus connecting said first and second I/O circuits.

145. (new) The electronic component of Claim 144, wherein said signal bus is used to transmit address signals.

146. (new) The electronic component of Claim 144, wherein said signal bus is used to transmit data signals.

147. (new) The electronic component of Claim 144, wherein said signal bus is used to transmit logic signals.

148. (new) The electronic component of Claim 144, wherein said signal bus is used to transmit analog signals.

149. (new) The electronic component of Claim 144, wherein said signal bus is used to transmit clock signals.

150. (new) The electronic component of Claim 144, wherein said signal bus is used to transmit a power voltage.

151. (new) The electronic component of Claim 144, wherein said signal bus is used to transmit a ground voltage.

152. (new) The electronic component of Claim 140 further comprising an external connection connected to said second I/O circuit.

153. (new) The electronic component of Claim 152 further comprising an ESD circuit connected to said external connection.

154. (new) The electronic component of Claim 140 is a semiconductor chip.

155. (new) The electronic component of Claim 140 is a semiconductor wafer.

156. (new) The electronic component of Claim 140, wherein said first I/O circuit comprises a receiver.

157. (new) The electronic component of Claim 140, wherein said first I/O circuit comprises a driver.

158. (new) The electronic component of Claim 140, wherein said second I/O circuit comprises a receiver.

159. (new) The electronic component of Claim 140, wherein said second I/O circuit comprises a driver.

160. (new) A method of fabricating an electronic component, comprising:

providing a semiconductor wafer comprising multiple I/O circuits, an interconnecting structure and a passivation layer, said passivation layer being over said interconnecting structure; and

forming an upper interconnecting structure over said passivation layer, wherein said upper interconnecting structure connects said multiple I/O circuits.

161. (new) The method of Claim 160, wherein said passivation layer comprises a topmost nitride layer.

162. (new) The method of Claim 160, wherein said passivation layer comprises a topmost oxide layer.

163. (new) The method of Claim 160, wherein said passivation layer comprises a topmost insulating layer formed using a CVD process.

164. (new) The method of Claim 160, wherein said multiple I/O circuits comprise a receiver.

165. (new) The method of Claim 160, wherein said multiple I/O circuits comprise a driver.

166. (new) A method of fabricating an electronic component, comprising:

providing a semiconductor wafer comprising a semiconductor circuit, a first I/O circuit, a second I/O circuit, an interconnecting structure and a passivation layer, said interconnecting structure connecting said first I/O circuit and said semiconductor circuit, said passivation layer being over said interconnecting structure; and

forming an upper interconnecting structure over said passivation layer, wherein said upper interconnecting structure connects said first and second I/O circuits.

167. (new) The method of Claim 166, wherein said passivation layer comprises a topmost nitride layer.

168. (new) The method of Claim 166, wherein said passivation layer comprises a topmost oxide layer.

169. (new) The method of Claim 166, wherein said passivation layer comprises a topmost insulating layer formed using a CVD process.

170. (new) The method of Claim 166, wherein said multiple I/O circuits comprise a receiver.

171. (new) The method of Claim 166, wherein said multiple I/O circuits comprise a driver.